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Image Edge Detection Using FPGA

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ABSTRACT—

Medical imaging often involves the injection of contrast agents and subsequent analysis of tissue enhancement patterns. X-ray angiograms are projections of 3D reality into 2D representations, there is a fair amount of self occlusion among the vessels, hence one cannot extract the vessels directly using the image intensities or gradients (edge) alone. Vessels extraction from angiogram images is useful for blood vessels measurement and computer visualizations of the coronary artery. This project describes the algorithm for automatic segmentation of coronary arteries in digital X-ray projections here an improved k-means algorithm is proposed. The performance of the proposed algorithm is compared with other techniques.

A methodology for implementing real-time DSP applications on a field programmable gate arrays (FPGA) using Xilinx System Generator (XSG) for Mat lab is presented in this paper. It presents the architecture for Edge Detection using Sobel Filter for image processing using Xilinx System Generator. The design was implemented targeting a Spartan3 a DSP 3400 device (XC3SD3400A-4FGG676C) then a vertex 5 (xc5vlx50-1ff676) .the edge detection methods has been verified successfully with no visually perceptual errors in the resulted images.

Index Terms— Edge detection, Hardware/software co-simulation, Image processing, System generator, Sobel edge detector.

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1.INTRODUCTION

The emerging market for video processing systems requires high-performance digital signal processing as well as low device costs appropriate for a volume application. Xilinx FPGA devices provide a platform with which to meet these two contrasting requirements. A Xilinx tool, the System Generator for DSP offers an efficient and straightforward method for transitioning from a PC-based model in Simulink to a real-time FPGA based hardware implementation. The system model can be simulated in the Simulink environment. This higher abstraction level reduces the analysis and debugging time. For real hardware testing, Xilinx System Generator supports the possibility to perform hardware in-the-loop co-simulation. This methodology provides easier hardware verification and implementation compared to HDL based approach. The Simulink simulation and hardware-in-the loop approach presents a far more cost efficient solution than other methodologies. The ability to quickly and directly realize a control system design as a real-time embedded system greatly facilitates the design process.

The goal of this project was to implement an image processing algorithm applicable to Edge Detection system in a Xilinx FPGA using System Generator for DSP, with a focus on achieving overall high performance, low cost and short development time.

2. LITERATURE SURVEY.

Cemilkirbas and Francis K.H. Quek,"A Review of Vessel Extraction Techniques and Algorithms", Technical Report. Vision Interfaces and Systems Laboratory (VLSI Lab),Department of Computer Science and Engineering, Write State University,Dayton,Ohio,Nov,2002.This Paper describes about various methods of vessel extraction techniques like pattern recognition approaches, model based approaches, tracking based approaches, artificial intelligence based approaches, neural network based approaches and miscellaneous tube like object detection approaches.Fezzan and J.C.Klein,"Robust Segmentation Of Vessels from retinal angiography", in IEEE International Conference on Digital Signal Processing ,Vol.2,pp. 1087-1090,1997.This paper explains the need for pre-processing of segmentation of angiograms images.Guo and P.ricjardson.,"Automatic vessel extraction from angiogram images", IEEE Computers in cardiology,Vol. 25, pp. 441-444, 1998.this paper explains the detail about balancing and smoothening of angiograms by median filter and projective non-linear diffusion method.

Yu-Fang;Jia-LiMao;Zhong-YangXiong,"An efficient clustering algorithm "International Conference on Machine Learning and Cybernetics,2003 Volume 1,2-5 Nov.2003 page(S):261- 265 Vol.1.This paper presents the overall idea of k means and deal with massive data, An improved K-means algorithm is also presented. it can avoid getting into locally optimal solution in some degree, and reduce the probability of dividing one big cluster into two or more ones owing to the adoption of squared-error criterion. UsamaFayyad,CoryReina, P.S.Bradeley Intialization of Iterative Refinement Clustering Algorithms. Microsoft Research Technical Report MSR-TR-98-38, June 1998.This technical report deals with a procedure for computing a refined starting condition from a given one that is based on efficient technique for estimating the modes of a distribution.Singh M.Patel, Koala, D,; Kim, T."Segmentation Of Functional MRI by K-means Clustering" Nuclear Science, IEEE Transactions on Volume 43,Issue 3,Part 2, June 1996 Page(S):2030-2036.This paper presents the segmentation of Firm into gray matter and large veins the intensity, phase and temporal delay of activated pixels as three correlated parameters in gradient echo images.

FangYaun;Zeng-HuiMeng;Hong-XiaZhang;Chaun-rudong;"A new algorithm to get the initial centroids ".Proceedings of 2004 International Conference on "Machine learning and Cybernetics 2004 Volume 2,2004 page(S):1191-1193 Vol.2.This paper evaluates the distances between every pair of data-points, and then tries to find out those data-points which are similar and finally construct initial centroids according to these found data-points.Roux; Winch, D 'Survey Of Clustering Algorithms" IEEE Transactions on Neural Networks Volume 16,Issue 3,May 2005 Page(S):645-678.This paper discuss the details regarding series of steps, ranging from pre-processing and algorithm development, to solution validity and evaluation. Choosing appropriate and meaningful features can greatly reduce the burden of subsequent designs and result evaluations reflect the degree of confidence to which we can rely on the generated clusters.

3. PROBLEM STATEMENT

Effective edge detection is required for many important areas such as machine vision and automated interpretation systems and is often used as the front end processing stage in project recognition and interpretation systems. An edge detector is defined as a mathematical operator of small spatial extent that responds in some way to these discontinuities usually classifying every image pixel as either belonging to an edge or not. Traditional image edge detectors commonly extract edges by adopting specific templates or in combination with smoothing functions. However traditional edge filtering methods often results in some drawbacks like broken edges, thick edges and false edges therefore many methods have been proposed to link these broken edges in order to improve edge detection. In our proposed algorithm, sobel's edge detector filters are applied in the horizontal and vertical directions and Otsu's threshold is used to determine edge or non edge pixels, and then on the output image a thinning process is applied to smooth the thick edges.

The visual result of the comparison of the results of the proposed algorithm with the results of the existed algorithm shows the effectiveness of the proposed algorithm.The algorithms and concepts used to define the system are modelled using high level software languages like Mat lab, Simulink and C. The Xilinx's System Generator for DSP is a new tool. For Hardware Implementation traditionally we are using DSP processor, but those have less MAC capability, Low speed and it consumes high power. Three most frequently used edge detection methods are used for comparison. These are Roberts's edge detection, Sobel edge detection, Prewitt edge detection.

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3.1 Roberts Detection

The Roberts cross operator performs a simple, quick to compute,2-D spatial gradient measurement on an image, it thus highlights regions of high spatial frequency which often corresponded to edges. In its most common usage, the input to the operator is a greyscale image, as the output. Pixel value at each point in the output represents the estimated absolute magnitude of the spatial gradient of the input image at that point.

Figure.1.Roberts Mask.

G_x

+1	0
0	-1

G_y

0	+1
-1	0

3.2. The Prewitt Edge Detection

The Prewitt edge detector is an appropriate way to estimate the magnitude and orientation of an edge. Although differential gradient edge detection needs a rather time consuming calculation to estimate the orientation from the magnitudes in the X- and Y-directions, the compass edge detection obtains the orientation directly from the kernel with the maximum response. The prewitt operator is limited to 8 possible orientations, however experience shows that most direct orientation estimates are not much more accurate. This gradient based edge detector is estimated in the 3×3 neighbourhood for eight directions. The entire eight convolutions masks are calculated. One convolution mask is then selected, namely that with the largest module.

Figure.2.PrewittMask

-1	+1	+1
-1	-2	+1
-1	+1	+1

0^0

+1	+1	+1
-1	-2	+1
-1	-1	+1

45^0

3.3.The Sobel Detection

The Sobel Operator performs a 2-D spatial gradient measurement on an image and so emphasizes regions of high spatial frequency that correspond to edges. Typically it is used to find the approximate absolute gradient magnitude at each point in an input image .In theory at least, the operator consists of a pair of 3×3 convolution kernels as shown in figure 4.One Kernel is simply to the other rotated by 90^0.This is very similar to the Roberts Cross operator. The convolution masks of the sobel detector are given below.

Figure.3.Sobel Mask

G_x

-1	0	+1
-2	0	+2
-1	0	-1

G_y

+1	+2	+1
0	0	0
-1	-2	-1

4. PROPOSED SYSTEM.

The proposed Xilinx System Generator. is a System-level modelling tool for Xilinx that facilitates FPGA Hardware design. It extends Simulink In many ways to provide a modelling environment well suited for hardware design. The software automatically converts the high level system DSP block diagram to RTL. The result can be synthesized to Xilinx FPGA technology using ISE tools. All of the downstream FPGA implementation steps including synthesis and place and route are automatically performed to generate an FPGA programming file. The Goals of this paper have been the following

One goal has been to compile an introduction to the subject of segmentation of angiograms. There exist a number of studies of other algorithms, but complete treatments on a technical level are not as common. Material from papers, journals, and conference proceedings are used that best describe the various parts. Segmentation is done using clustering technique, which separates the vessel structure from background. There is no clustering algorithm that can be universally used to solve all problems. So the goal is to search for best algorithms that can be used to segment medical images. Second goal is to compare the performance with other segmentations approaches. A final goal has to design and implement a segmentation algorithm.

5. METHODS/SOLUTIONS.

5.1 System Generator Design Flow For Implementation On Fpga

The algorithms and concepts used to define the system are modelled using high level software languages like Mat lab, Simulink and C. The Xilinx's system generator for DSP is a new tool, which comes with a predefined block set along with Mat lab Simulink software packet and can be used to implement the algorithms. Mat lab is a high-level technical computing language and interactive environment for algorithm development, data visualization, data analysis, and numeric computation. In addition to the intellectual property functions provided in Mat lab, the software packet is uniquely adept with vector and array based waveform data at the core of algorithms, which is suitable for applications such as image and video processing. Mat lab-simulink is an environment for multi domain simulation and Model-Based design for dynamic and embedded systems. it provides an interactive graphical environment, event-driven simulator, and extensive library of parameterizable functions that allow design,simulate,implement,and test a variety of time-varying systems, including communications,controls,signal processing, image and video processing.Matlab-simulink is used in this application as the high level development tool in the design process.

The Xilinx's Generator is a system-level modelling tool from Xilinx that facilitates FPGA hardware design. It extends Simulink in many ways to provide a modelling environment well suited for hardware design. The software automatically converts the high level system DSP block diagram to RTL.The result can be synthesized to Xilinx's FPGA technology using ISE tools, all of the downstream FPGA implementation steps including synthesis and place and route are automatically performed to generate an FPGA programming file.System Generator automates the design process, debugs, and implements and verifies the Xilinx-based FPGAs.It provides a high speed HDL co-simulation interfaces which give up to a 1000x simulation performance increase. It also provide s a system integration platform for the design of DSP FPGAs that allows the RTL, Simulink ,Mat lab and C /C++ components of a DSP system to come together in a single simulation and implementation environment. System Generator supports a black box block that allows RTL to be imported into Simulink and co-simulated with either models or Xilinx ISE simulator.

5.2 Sobel Edge Detector

Edge detection is a fundamental tool used in most image processing applications to obtain information from the frames as a precursor step to feature extraction and object segmentation. This process detects outlines of an object and the background in the image. An edge detection filter can also be used to improve the appearance of blurred or anti-aliased video streams.Commonly used method for detecting edges is to apply derivative operators on images. Derivative based approaches can be categorized into two groups, namely first and second order derivative methods. First order derivative

based techniques depend on computing the gradient several directions and combining the result of each gradient. The value of the gradient magnitude and orientation is estimated using two differentiation masks.The Sobel edge detection algorithm uses a 3×3 table of pixels is called a convolution table, because it moves across the image in a convolution-style algorithm.

$$G_x(X, Y) = \begin{matrix} +1 & 0 & -1 \\ +2 & 0 & -2 \\ +1 & 0 & -1 \end{matrix} *I(X,Y) \qquad (1)$$

$$G_y(X, Y) = \begin{matrix} +1 & 0 & -1 \\ 0 & 0 & 0 \\ -1 & -2 & -1 \end{matrix} *I(X,Y) \qquad (2)$$

In each pixel (X, Y), the approximations of the horizontal and vertical gradients are combined as follows, to obtain an approximation of the gradient value.

$$G(X, Y) = \sqrt{(G_x(X,Y)^2)+G_y(X,Y)^2} \qquad (3)$$

$$G(X, Y)=|G_x(X,Y)|+|G_Y(X,Y)| \qquad (4)$$

The reason for using sobel operator is that it is insensitive to noise and it has relatively small masks than other operator such as Robert operator, two orders Palladian operator and others.

5.3 Comparison Of The Various Edge Detectors.

As edge detection is a fundamental step in computer vision, it is necessary to point out the true edges to get the best results from the matching process.

5.3.1 Classical (Sobel, Prewitt)

The primary advantages of the classical operator are simplicity. The Roberts cross operator provides a simple approximation to the gradient magnitude. The second advantages of the classical operator are detecting edges and their orientations is said to be simple due to the approximation of the gradient magnitude.

The disadvantages of these cross operator are sensitivity to the noise, in the detection of the edges and their orientations. The increase in the noise to the image will eventually degrade the magnitude of the edges. The major disadvantage is the inaccuracy, as the gradient magnitude of the edges decreases. Most probably the accuracy also decreases operator are detecting edges and their orientations. In this cross operator, the detection of the edges and their orientations is said to be simple due to the approximation of the gradient magnitude.

5.3.2 Zero Crossing (Laplacian)

The advantages of the zero crossing operators are detecting edges and their orientations. In this cross operator detection of the edges and their orientations is said to be simple due the approximation of the gradient magnitude is simple. The second advantage is the fixed characteristics in all directions. The disadvantage is sensitivity to noise. In detecting the edges and their orientations are increased in the noise to the images this will eventually degrade the magnitude of the edges. The second disadvantage is that the operation gets diffracted by some of the existing edges in the noise image.

5.3.3 Gaussian (Global Filter)

Global filter for edge detection is based on the frequency and orientation representations. Gabor filters are similar to those of the human perception system that is related to practically appropriate for texture representation and discrimination.2D Gabor filter is a Gaussian kernel function modulated by a sinusoidal plan wave. Gabor filters linked to Gabor wavelets. They can be designed for a number of dilations and rotations. In general, the expansion is not applied for Gabor wavelets. The needs are the computation of bi-orthogonal wavelets, which is very time-consuming. To overcome this problem the filter bank consisting of Gabor filters with various scales and rotations are created .The Gabor filters are convolved with the signal, resulting in so is called Gabor space, its advantages is Gabor function which is good fit to the receptive field weight functions. The Gabor filter is very useful in image processing applications using edge detection.

5.3.4 Gaussian (Canny)

The smoothing concept has been applied in this Gaussian operation, so the finding of errors is effective by using the probability. The next advantage is improving the signal with respect to noise ratio and this is established by No maxima suppression method as its results in one pixel wide ridges as output. The third advantage is Better detection of edges especially in noise state with the help of threshold method. The major disadvantage is the computation of the gradient calculation for generating the angle of suppression. The main disadvantage is time consumption because of complex computation.

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6. SIMULATIONS AND EXPERIMENT RESULTS.

6.1HARDWARE/SOFTWARE CO-SIMULATION IN SYSTEM GENERATOR

The System Generator Black Box block allows VHDL, Verilog, and EDIF to be brought into a design. The Black Box behaves like other system generator blocks. It is wired into the design, participates in simulations, and is compiled into hardware. System generator compiles a Black Box Block; it automatically wires the imported module and associated files into the surrounding net list. The Black Box block provides a way to incorporate hardware description language (HDL) models them into System Generator .The design of our architecture with Xilinx System Generator is shown in below "figure4". System generator simulates black boxes by automatically launching an HDL simulator, generating additional HDL as needed, compiling HDL, scheduling simulation events, and handling the exchange of data between the semolina and the HDL simulator. This is called HDL co-simulation. System Generator provides hardware co-simulation making it possible to incorporate a design running in an FPGA directly into a simulation."Hardware Co-Simulation" compilation targets automatically

Figure 4: System Generator Project for simulation

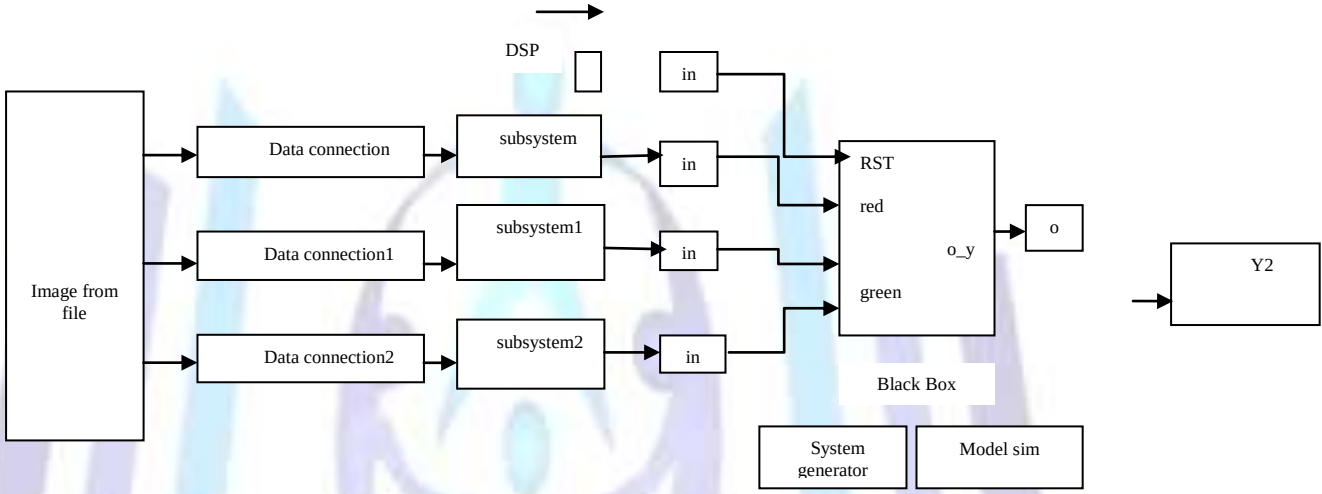
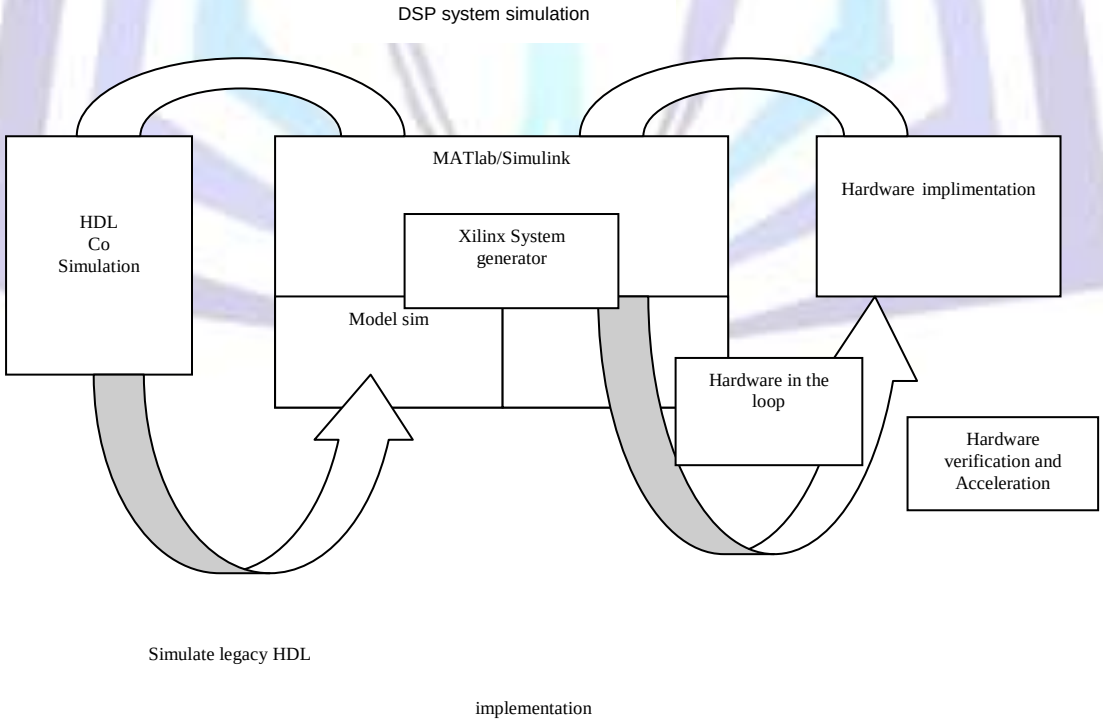


Figure 5:FPGA based Hardware-Software Co-Simulation.



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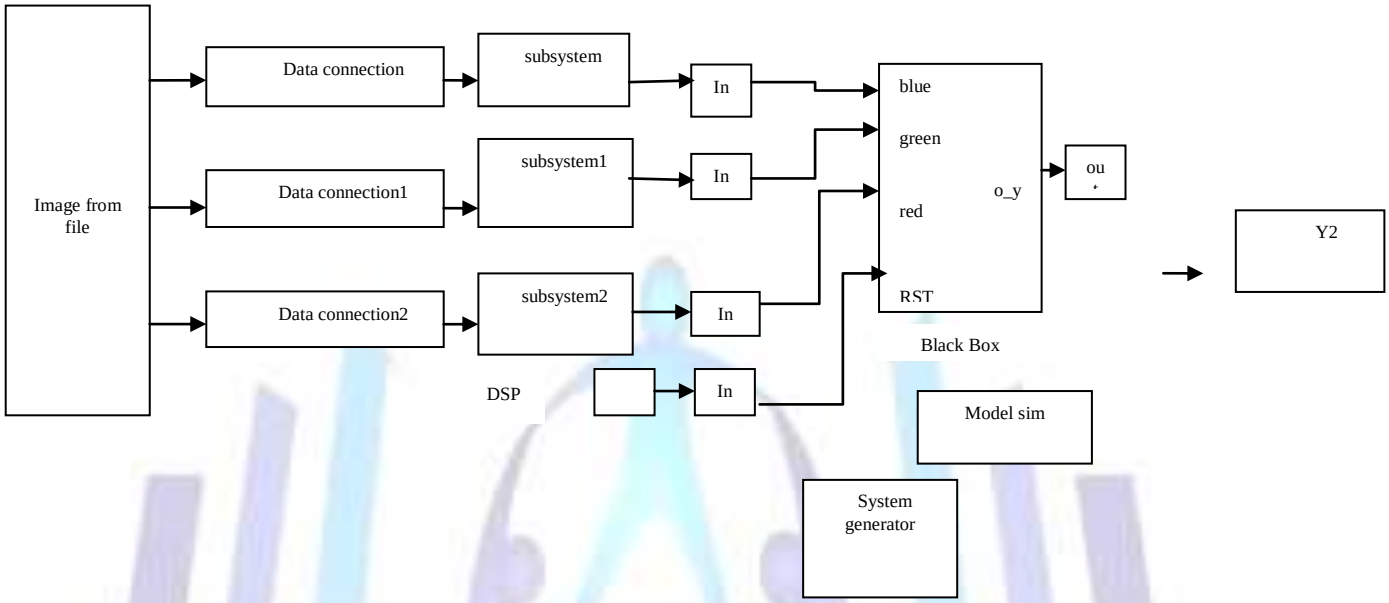
create a bit stream and associate it to a block shown in below “fig.5”. When the system design is simulated in simulink, results for the compiled portion are calculated in actual FPGA hardware, often resulting in significantly faster simulation times while verifying the functional correctness of the

hardware. System Generator for DSP supports Ethernet as well as JTAG communication between a hardware platform and simulink.

Figure 6: system generator project for hardware-in-the-loop testing on Virtex5 platform.



System generator provides a generic interface that uses JTAG and a Xilinx programming

cable to communicate with FPGA hardware “fig.6” shows the model with the JTAG-based hardware co-simulation block implemented on vertex 5 platforms. Point to point Ethernet co-simulation provides a straightforward high performance co-simulation environment using a direct, point to point Ethernet connection between a PC and FPGA platform. The target FPGA chip is Xilinx Spartan 3 a DSP 3400 XC3SD3400A-4FGG676C and vertex 5 xc5vlx50-1ff676.The optimization setting is for maximum clock speed. Table 1 details the resource requirements of the design. To provide performance evaluation, the implemented sobel edge detector architecture using low cost available Spartan 3 development system with Xilinx chip XC3S50 -5PQ208.The properties of other designs along with ours are listed in Table 2.As seen from this table, the design of the sobel edge detector proposed by requires 204 CLB on the basis clock rate of 134.756 MHz On the other hand ,our resulting architecture spent about 177 CLB with a working frequency up to 54.505 Mhz.Obviously,the proposed architecture has lower complexity and improved efficiency in area, thus providing a good choice in terms of low cost hardware.

Table 1: FPGA resources used in the implementation for the Sobel Edge Detector

	Spartan 3A DSP 3400			Vertex 5 xe5vlx50-1ff676		
	used	available	%	used	available	%
Number of slice Registers	2302	23872	9%	1798	28800	6%
Number of slice LUTs	1755	47744	3%	2299	28800	7%
Number of LUT-FF pairs	3023	47744	6%	370	3727	9%
Number of bonded IOBs	34	469	7%	34	440	7%
Number of BUFG/BUFGCT	1	24	4%	1	32	3%
Number of DSP48s	3	126	2%	-	-	-%
Maximum Frequency	59.25 MHZ			103.616 MHZ		

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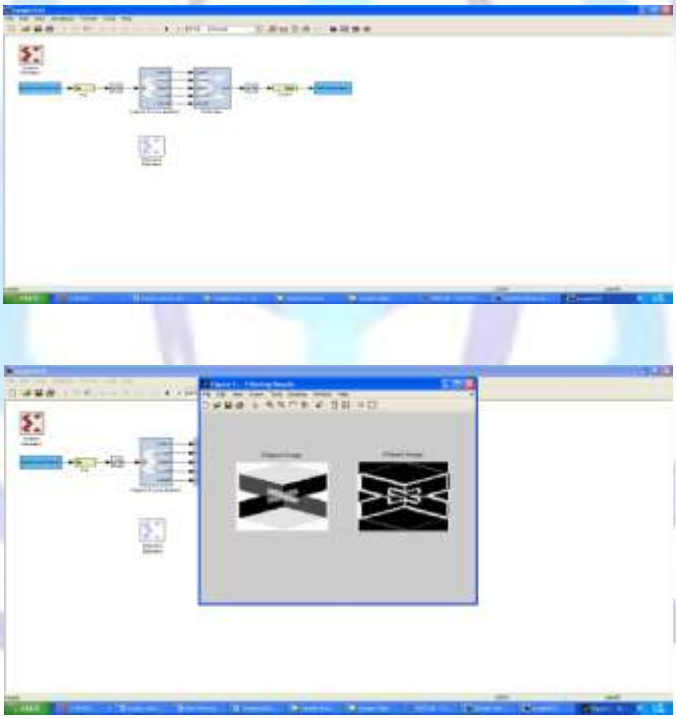
Table 2: Performance Comparison

	Our design			Design		
	used %	available		used %	available	
Number of slices	177	768	23%	204	768	26%
Number of slice Flip Flop	401	1536	26%	280	1536	18%
Number of 4 input LUT	277	1536	18%	202	1536	13%
Number of bonded IOBS	34	124	27%	81	124	65%
Number of GCLKS	1	8	12%	1	8	12%
Maximum Frequency	54.505 MHZ			134.756 MHZ		

. **Figure 7: Outputs from different implementation.**



7. CONCLUSION&FUTURE WORK.

Xilinx system generator has a unique hardware in the loop co-simulation feature that allows designers to greatly accelerate simulation while simultaneously verifying the design in hardware. The purpose of this paper was to demonstrate the use of system generator to design a system edge detection for image processing .this design is implemented in the device Spartan 3A DSP 3400(XC3SD3400A-4FGG676C) and vertex 5(xc5vlx50-1ff676). The implemented sobel edge detector architecture using low cost available Spartan 3 development system with Xilinx chip XC3S50-5PQ208 has 54.505 MHz maximum frequency and uses 177 CLB slices with 23%utilization, so there is possibility of implementing some more parallel processes with this architecture on the same FPGA. Future works include the use of the Xilinx System Generator development tools for the implementation of other blocks used in computer vision like feature extraction and object detection on Xilinx programmable Gate Arrays(FPGA).

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